



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Applicant: Sunil Talwar et al.

Title: LOGIC CIRCUIT AND METHOD FOR CARRY AND SUM GENERATION AND METHOD OF DESIGNING SUCH A LOGIC CIRCUIT

Docket No.: 1365.063US1

Serial No.: 10/714,408

Filed: November 14, 2003

Examiner: Unknown

Group Art Unit: 2124

Mail Stop Amendment

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450


We are transmitting herewith the following attached items (as indicated with an "X"):

- ☒ Return postcard.
- ☒ Supplemental Information Disclosure Statement (2 pgs.), Form 1449 (2 pgs.), and copies of 12 cited documents.

Please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.


Customer Number 21186

By: 
Atty: Timothy B. Chise
Reg. No. 40,957

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 10 day of February, 2006.



Name



Signature

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
(GENERAL)



10/714,408

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Sunil Talwar et al.	Examiner:	Unknown
Serial No.:	10/714,408	Group Art Unit:	2124
Filed:	November 14, 2003	Docket:	1365.063US1
Title:	LOGIC CIRCUIT AND METHOD FOR CARRY AND SUM GENERATION AND METHOD OF DESIGNING SUCH A LOGIC CIRCUIT		

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicants respectfully request that this Supplemental Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicants request that a copy of the 1449 form, initialed as being considered by the Examiner, be returned to the Applicants with the next official communication.

Pursuant to 37 C.F.R. §1.97(b), it is believed that no fee or statement is required with the Supplemental Information Disclosure Statement. However, if an Office Action on the merits has been mailed, the Commissioner is hereby authorized to charge the required fees to Deposit Account No. 19-0743 in order to have this Supplemental Information Disclosure Statement considered.

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Serial No :10/714,408

Filing Date: November 14, 2003

Title: LOGIC CIRCUIT AND METHOD FOR CARRY AND SUM GENERATION AND METHOD OF DESIGNING SUCH A LOGIC CIRCUIT

Page 2

Dkt: 1365.063US1

Pursuant to 37 C.F.R. 1.98(a)(2), Applicant believes that copies of cited U.S. Patents and Published Applications are no longer required to be provided to the Office. Notification of this change was provided in the United States Patent and Trademark Office OG Notices dated October 12, 2004. Thus, Applicant has not included copies of any US Patents or Published Applications cited with this submission. Should the Office require copies to be provided, Applicant respectfully requests that notice of such requirement be directed to Applicant's below-signed representative. Applicant acknowledges the requirement to submit copies of foreign patent documents and non-patent literature in accordance with 37 C.F.R. 1.98(a)(2).

The Examiner is invited to contact the Applicants' Representative at the below-listed telephone number if there are any questions regarding this communication.

Respectfully submitted,
SUNIL TALWAR ET AL.

By their Representatives,
SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 349-9587

Date

9 Feb '06

By

Timothy B Clise


Reg. No. 40,957

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Name

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Substitute for form 1449A/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)



Complete if Known

Application Number	10/714,408
Filing Date	November 14, 2003
First Named Inventor	Talwar, Sunil
Group Art Unit	2124
Examiner Name	Unknown

Sheet 1 of 2

Attorney Docket No: 1365.063US1

US PATENT DOCUMENTS

Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Filing Date If Appropriate
	US-2003/0016055A1	01/23/2003	Oodaira, N., et al.	06/18/2002
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	US-6,598,061	07/22/2003	Symes, D. H., et al.	06/15/2000
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	US-6,938,061	08/30/2005	Rumynin, D., et al.	08/11/2000

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	T ²
	EP-0947914A1	10/06/1999	McGregor, M. S.	
	GB-2318892	05/06/1998	Hobson, R. D., et al.	
	WO-03052583A2	06/26/2003	Meulemans, P., et al.	

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		"Communication Pursuant to Article 96(2) EPC, for application No. EP 02 722 402.1, date mailed June 6, 2005", 3 Pages	
		ELDRIDGE, S. E., et al., "Hardware Implementation of Montgomery's Modular Multiplication Algorithm", <u>IEEE Transactions on Computers</u> , 42(6), (1993), 693-699	
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		MARNANE, W. P., "Optimised Bit Serial Modular Multiplier for Implementation on Field Programmable Gate Arrays", <u>Electronics Letters</u> , 34(8), (1998), 738-739	
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EXAMINER**DATE CONSIDERED**

Substitute Disclosure Statement Form (PTO-1449)

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.¹ Applicant's unique citation designation number (optional) ² Applicant is to place a check mark here if English language Translation is attached

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Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>	<i>Complete if Known</i>	
	Application Number	10/714,408
	Filing Date	November 14, 2003
	First Named Inventor	Talwar, Sunil
	Group Art Unit	2124
	Examiner Name	Unknown
Sheet 2 of 2	Attorney Docket No: 1365.063US1	

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		SONG, PAUL J., et al., "Circuit and Architecture Trade-offs for High-Speed Multiplication", <u>IEEE Journal of Solid-State Circuits</u> , Vol. 26, No. 9, (September 1991), 1184-1198	
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EXAMINER

DATE CONSIDERED

Substitute Disclosure Statement Form (PTO-1449)

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 809. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.¹ Applicant's unique citation designation number (optional) : Applicant is to place a check mark here if English language Translation is attached